We Claim:

1. A self-test circuit, comprising:

an address generator circuit for generating a test address for testing a memory circuit;

a control circuit connected to said address generator circuit for controlling said address generator circuit, said control circuit having signal inputs for receiving test commands; and

a register storing an address difference value and connected to said control circuit and to said address generator circuit, upon receiving a first test command said control circuit driving said address generator circuit to increase the test address by the address difference value in an event of a subsequent memory access, upon receiving a second test command said control circuit driving said address generator circuit to decrease the test address by the address difference value in an event of the subsequent memory access.

2. The self-test circuit according to claim 1, wherein said control circuit writes the address difference value to said first register with an aid of a programming command.

3. The self-test circuit according to claim 1, further comprising:

a further register storing a further address difference value and connected to said control circuit and to said address generator circuit, upon receiving a third test command said control circuit driving said address generator circuit to increase the test address by the further address difference value in an event of the subsequent memory access, upon receiving a fourth test command said control circuit driving said address generator circuit to decrease the test address by the further address difference value in an event of the subsequent memory access.

4. The self-test circuit according to claim 3, wherein said control circuit writes the further address difference value to said further register with an aid of a further programming command.

5. The self-test circuit according to claim 1, wherein said address generator unit has an adder unit and a subtractor unit, each of which can be activated depending on the test commands.

6. The self-test circuit according to claim 1, wherein said control circuit starts a generation of the test address by said address generator unit in dependence on a start command.

7. A method for testing a memory circuit having a self-test circuit, which comprises the steps of:

writing an address difference value to a first register;

increasing a test address by the address difference value in an event of a subsequent memory access upon receiving a first test command; and

decreasing the test address by the address difference value in an event of the subsequent memory access upon receiving a second test command.

8. The method according to claim 7, which further comprises applying the first test command and the second test command successively to jump back and forth between two test addresses.

9. The method according to claim 7, which further comprises applying a start command to the self-test circuit to start testing of the memory circuit by the self-test circuit.

10. A method for testing a memory circuit having a self-test circuit, which comprises the steps of:

writing a first address difference value to a first register;

increasing a test address by the first address difference value in an event of a subsequent memory access upon receiving a first test command;

decreasing the test address by the first address difference value in an event of the subsequent memory access upon receiving a second test command;

writing a second address difference value to a second register;

increasing the test address by the second address difference value in an event of the subsequent memory access upon receiving a third test command; and

decreasing the test address by the second address difference value in an event of the subsequent memory access upon receiving a fourth test command.

11. The method according to claim 10, which further comprises applying the first test command, the third test command, the fourth test command and the second test command successively to jump back and forth between the four test addresses.

12. The method according to claim 10, which further comprises applying a start command to the self-test circuit to start testing of the memory circuit by the self-test circuit.